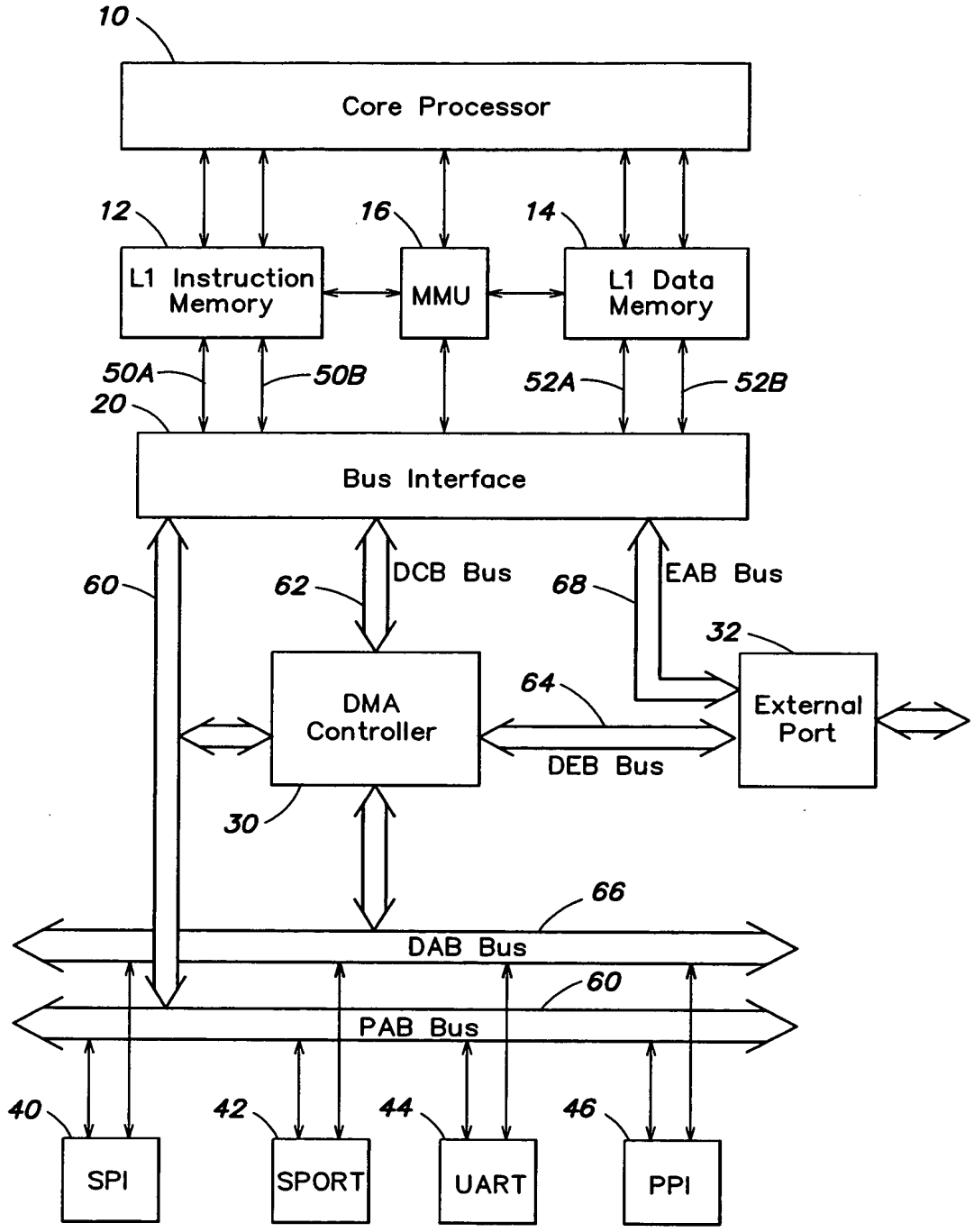

FIG. 1

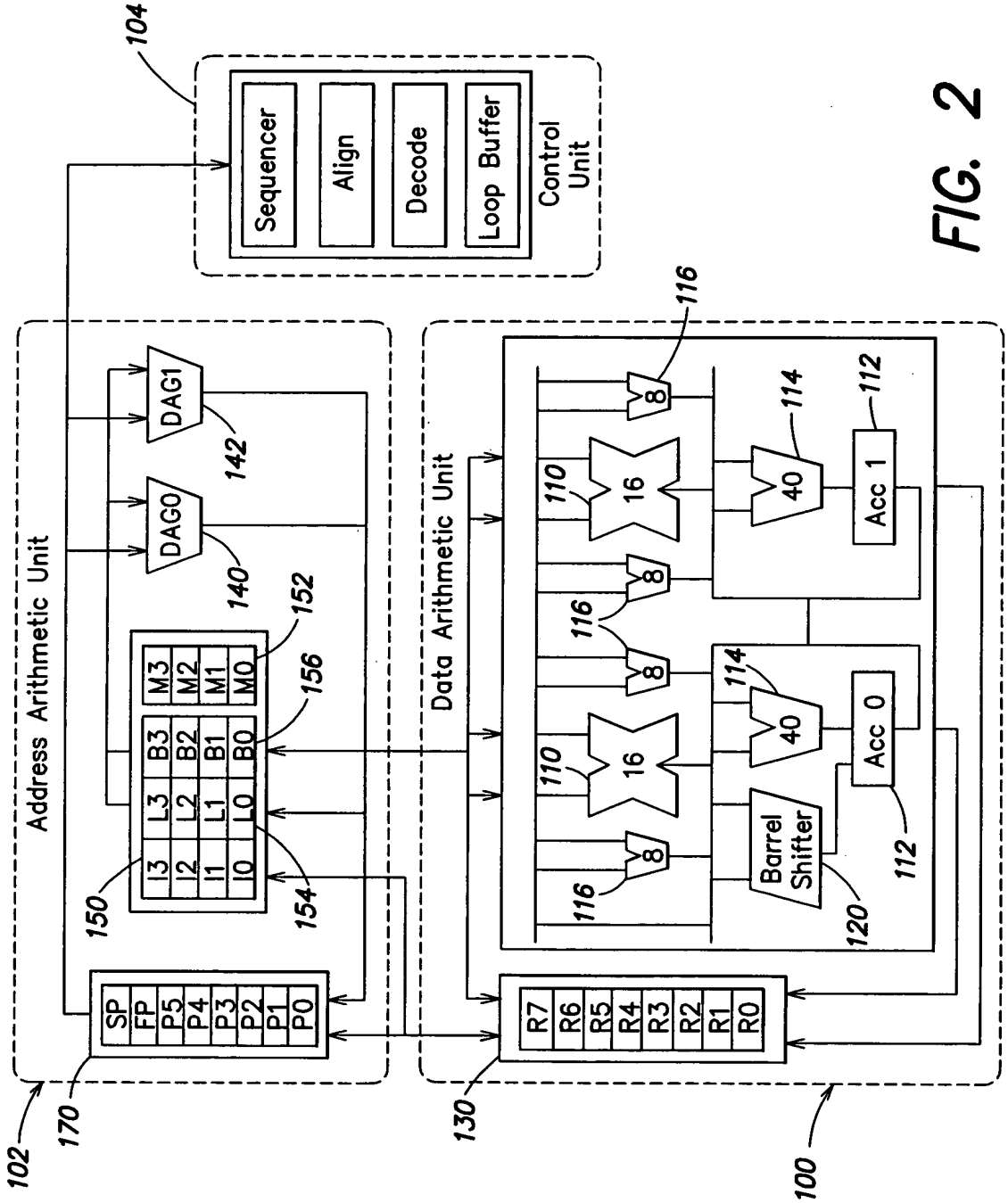
104
Sequencer
Align
Decode
Loop Buffer
Control Unit
Address Arithmetic Unit
DAG1
DAG0
142
140
152
156
M3
M2
M1
M0
B3
B2
B1
B0
L3
L2
L1
L0
I3
I2
I1
I0
150
154
SP
FP
P5
P4
P3
P2
P1
P0
170
102
Data Arithmetic Unit
116
110
16
8
114
40
112
Acc 1
Acc 0
Barrel Shifter
120
R7
R6
R5
R4
R3
R2
R1
R0
130
100

FIG. 2

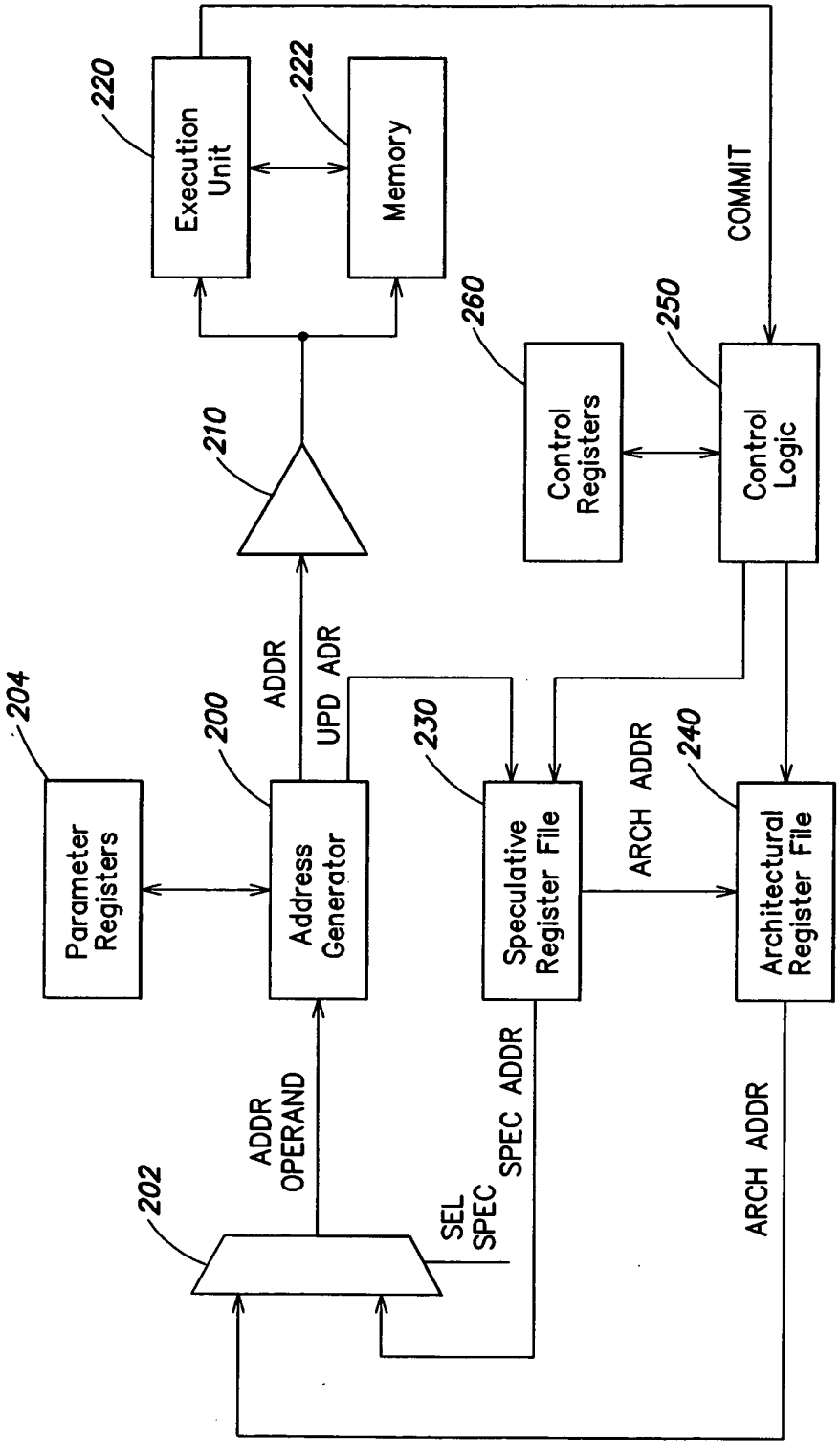
220
Execution Unit
222
Memory
COMMIT
260
Control Registers
250
Control Logic
210
204
200
ADDR
UPD ADR
230
240
Parameter Registers
Address Generator
Speculative Register File
ARCH ADDR
Architectural Register File
ADDR OPERAND
SPEC ADDR
202
SEL SPEC
ARCH ADDR

FIG. 3

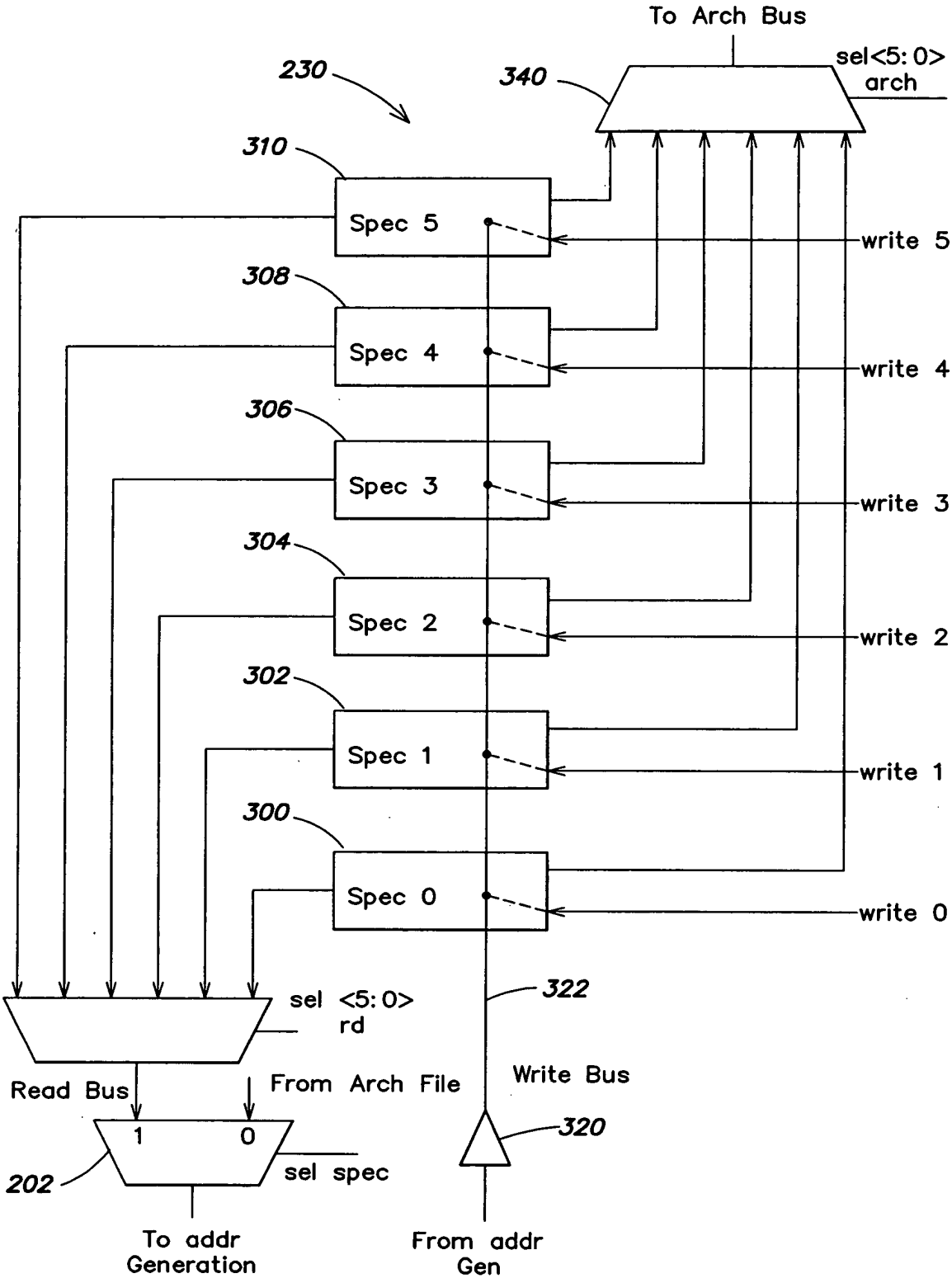
To Arch Bus
230
340
sel<5:0>
arch
310
Spec 5
write 5
308
Spec 4
write 4
306
Spec 3
write 3
304
Spec 2
write 2
302
Spec 1
write 1
300
Spec 0
write 0
322
sel <5:0>
rd
Read Bus
From Arch File
Write Bus
320
1
0
202
sel spec
To addr
Generation
From addr
Gen

FIG. 4

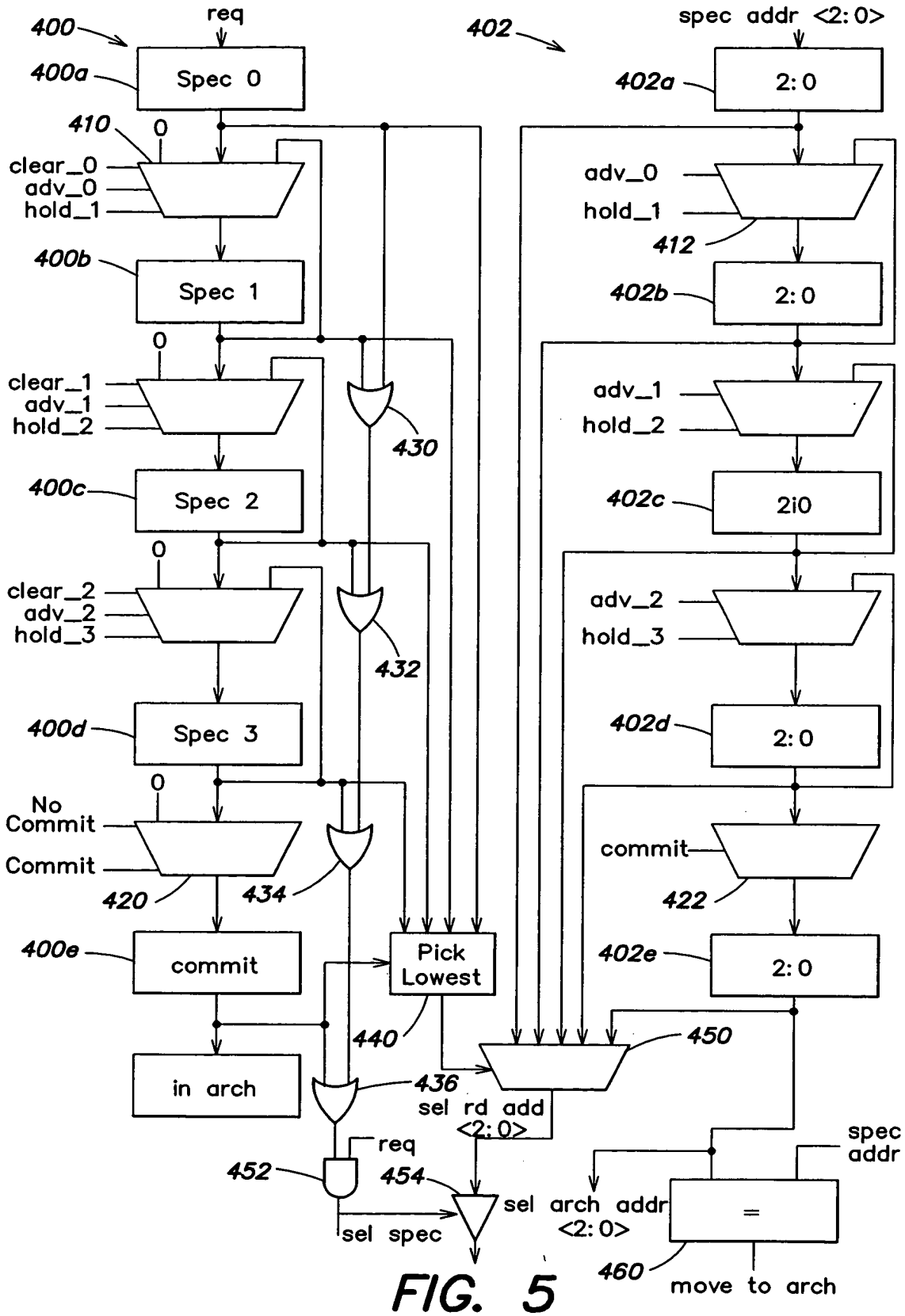
400
req
Spec 0
400a
410
0
clear_0
adv_0
hold_1
400b
Spec 1
clear_1
adv_1
hold_2
430
400c
Spec 2
clear_2
adv_2
hold_3
432
400d
Spec 3
No Commit
Commit
420
434
400e
commit
in arch
Pick Lowest
440
436
452
req
454
sel spec
402
spec addr <2:0>
402a
2:0
adv_0
hold_1
412
402b
2:0
adv_1
hold_2
402c
2i0
adv_2
hold_3
402d
2:0
commit
422
402e
2:0
450
sel rd add <2:0>
sel arch addr <2:0>
=
spec addr
460
move to arch

FIG. 5

Example 0

```
A    ro = [I0 ++ M0]
B    ro = [I0 ++ M0]
C    ro = [I0 ++ M0]
D    ro = [I0 ++ M0]
E    ro = [I0 ++ M0]
F    ro = [I0 ++ M0]
G    ro = [I0 ++ M0]
```

FIG. 6

INSTR A IO

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x0
Spec 1	0	0xX
Spec 2	0	0xX
Spec 3	0	0xX
Commit	0	0xX

400 402

SPEC RF

0	A
1	–
2	–
3	–
4	–
5	–

230

FIG. 7A

INSTR B IO

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x1
Spec 1	1	0x0
Spec 2	0	0xX
Spec 3	0	0xX
Commit	0	0xX

400 402

SPEC RF

0	A
1	B
2	–
3	–
4	–
5	–

230

FIG. 7B

INSTR C IO

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x2
Spec 1	1	0x1
Spec 2	1	0x0
Spec 3	0	0xX
Commit	0	0xX

400 402

SPEC RF

0	A
1	B
2	C
3	–
4	–
5	–

230

FIG. 7C

INSTR D IO

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x3
Spec 1	1	0x2
Spec 2	1	0x1
Spec 3	1	0x0
Commit	0	0xX

400 402

SPEC RF

0	A
1	B
2	C
3	D
4	–
5	–

230

FIG. 7D

INSTR E IO

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x4
Spec 1	1	0x3
Spec 2	1	0x2
Spec 3	1	0x1
Commit	1	0x0

400 402

SPEC RF

0	A
1	B
2	C
3	D
4	E
5	–

230

FIG. 7E

INSTR F IO

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x5
Spec 1	1	0x4
Spec 2	1	0x3
Spec 3	1	0x2
Commit	1	0x1

400 402

SPEC RF

0	–
1	B
2	C
3	D
4	E
5	F

230

FIG. 7F

INSTR G IO

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x0
Spec 1	1	0x5
Spec 2	1	0x4
Spec 3	1	0x3
Commit	1	0x2

SPEC RF

0	G
1	–
2	C
3	D
4	E
5	F

230

FIG. 7G

Example 1

```
A    r0 = [P0 ++]
B    r1 = [P1 ++]
C    r2 = [P1 ++]
D    r3 = [P1 ++]
E    r4 = [P1 ++]
F    r5 = [P1 ++]
G    r6 = [P1 ++]
```

FIG. 8

P0

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x0
Spec 1	0	0xX
Spec 2	0	0xX
Spec 3	0	0xX
Commit	0	0xX

440 442

SPEC RF

	A
0	
1	–
2	–
3	–
4	–
5	–

230

P1

Stage	In Spec Reg	ADDR Reg
Spec 0	0	0xX
Spec 1	0	0xX
Spec 2	0	0xX
Spec 3	0	0xX
Commit	0	0xX

450 452

INSTR A

FIG. 9A

P0

Stage	In Spec Reg	ADDR Reg
Spec 0	0	0xX
Spec 1	1	0x0
Spec 2	0	0xX
Spec 3	0	0xX
Commit	0	0xX

440 442

SPEC RF

0	A
1	B
2	–
3	–
4	–
5	–

230

P1

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x1
Spec 1	0	0xX
Spec 2	0	0xX
Spec 3	0	0xX
Commit	0	0xX

450 452

INSTR B

FIG. 9B

P0

Stage	In Spec Reg	ADDR Reg
Spec 0	0	0xX
Spec 1	0	0xX
Spec 2	1	0x0
Spec 3	0	0xX
Commit	0	0xX

440 442

SPEC RF

0	A
1	B
2	C
3	–
4	–
5	–

230

P1

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x2
Spec 1	1	0x1
Spec 2	0	0xX
Spec 3	0	0xX
Commit	0	0xX

450 452

INSTR C

FIG. 9C

P0

Stage	In Spec Reg	ADDR Reg
Spec 0	0	0xX
Spec 1	0	0xX
Spec 2	0	0xX
Spec 3	1	0x0
Commit	0	0xX

440 442

SPEC RF

0	A
1	B
2	C
3	D
4	–
5	–

230

P1

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x3
Spec 1	1	0x2
Spec 2	1	0x1
Spec 3	0	0xX
Commit	0	0xX

450 452

INSTR D

FIG. 9D

P0

Stage	In Spec Reg	ADDR Reg
Spec 0	0	0xX
Spec 1	0	0xX
Spec 2	0	0xX
Spec 3	0	0xX
Commit	1	0x0

440 442

SPEC RF

0	A
1	B
2	C
3	D
4	E
5	–

230

P1

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x4
Spec 1	1	0x3
Spec 2	1	0x2
Spec 3	1	0x1
Commit	0	0xX

450 452

INSTR E

FIG. 9E

P0

Stage	In Spec Reg	ADDR Reg
Spec 0	0	0xX
Spec 1	0	0xX
Spec 2	0	0xX
Spec 3	0	0xX
Commit	0	0xX

440 442

SPEC RF

0	–
1	B
2	C
3	D
4	E
5	F

230

P1

Stage	In Spec Reg	ADDR Reg
Spec 0	1	0x5
Spec 1	1	0x4
Spec 2	1	0x3
Spec 3	1	0x2
Commit	1	0x1

450 452

INSTR F

FIG. 9F